# PRACTICAL DESIGN TECHNIQUES FOR SOLID STATE MICROWAVE GENERATORS

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In a harmonic generator, the following principles constitute desirable design criteria: 1) Provide an impedance match at the input; 2) provide an impedance match at the output; 3) prevent the output from reaching the generator; 4) prevent the input from reaching the load; 5) prevent other harmonic currents from flowing except in reactive idler terminations; and 6) operate the diode at the optimum point on its capacitance-voltage characteristic.

An optimum bias point of approximately $V_b/3$ has been observed empirically for both abrupt and graded junction diodes and represents a good design point. For high frequency operation, it is desirable to use a diode having a high cutoff frequency. The power handling capability is proportional to the capacitance of a diode and to its breakdown voltage squared. A compromise must be made that will allow a high cutoff frequency and a large enough breakdown voltage to handle the expected power.

A standard circuit is shown in Fig. 1. For the doubler*, the capacitance of the diode at $V_b/3$ is $C_o$. The inductance $L_o$ resonates the diode capacitance at the geometric mean frequency of the input and output which is $\sqrt{2}\omega$. An input trap prevents second harmonic power from reaching the generator. An output trap prevents the fundamental power from reaching the load. The input circuit is series resonant at $\omega$, and the output circuit is series resonant at $2\omega$. This leaves only a pure resistance to be matched to the generator and load. The inductance in series with the diode also presents a high impedance to other harmonics. For

*A.T. Fisher "Capacity Diode Parametric Performance & Circuit Design by a Finite Currents Method", Redstone Arsenal Report No. DG-7R-1-59, January, 1959

tripler and quadrupler operation, the shunt arm is modified to be two paths, both of which are resonant at the second harmonic idler frequency. Thus an idler path is provided around the loop. Because of nonlinearity, the exact value of the input and output resistance to be matched is unknown. As a starting point, the input and output matching networks can be designed to match the spreading resistance of the diode and then adjusted for optimum power and efficiency.

A coaxial doubler is shown in Fig. 2A. The input $\lambda/4$ short stub is an open to frequency $\omega$ and a short to frequency $2\omega$. The output $\lambda/4$ open stub is an open to $2\omega$ and a short for $\omega$. The matching networks cancel the varactor reactance and transform the input and output resistances. A coaxial quadrupler is shown in Fig. 2B. The $\lambda/4$ short circuited stub is an open circuit for the fundamental and a short circuit for the second and fourth harmonics. The $\lambda/4$ open stub is a short circuit to the fundamental and an open circuit to the fourth harmonic. The $\lambda/8$ open stub is a short circuit to the second harmonic idler and an open circuit to the fourth harmonic.

If a carrier signal and a spurious signal are both impressed upon a multiplier, the output will contain the desired frequency and a new spurious signal which has the original frequency separation from the carrier. The degradation in relative amplitude of the original carrier with respect to the spurious signal that occurs is known as spurious enhancement. It can be shown that spurious enhancement will be equal to 20 log R (db) where R is the multiplication ratio.

Relaxation modes have sometimes been difficult to suppress in high power multipliers. The relaxation oscillation occurs in the varactor bias circuit under large signal conditions and modulates the output. Another observed property is the hysteresis tuning effect. This effect is due to the nonlinear change in capacitance of the diode with RF drive. All of these problems have been solved through tuning or bias adjustment.

The criteria for a complete multiplier system are obtained from the follow-

ing factors: 1) Output frequency; 2) output power; 3) output bandwidth; and 4) spectrum purity required. The output frequency fixes the cascaded multiplying ratio. For doublers, triplers and quadruplers, TABLE I gives the multiplying ratios. The output power from the cascade will be a function of the individual multiplier efficiencies and the available power at the input frequency. TABLE II presents a large number of solid-state multiplier results which may be helpful. The conversion losses of TABLE II have been plotted versus frequency in Fig. 3. The bandwidth of a multiplier is a function of the circuitry in which it is used. With the circuits given, the parametric multiplier cascade is a narrow band device (<1%) unless the designer is willing to sacrifice efficiency.

The individual multiplier units must be capable of operating over the necessary input power range, and be tuned so that no detrimental relaxation modes exist over this range. The spurious levels are determined by the output purity desired. If the multiplier is followed by others, then the expected spurious enhancement must be considered in specifying individual purity requirements.

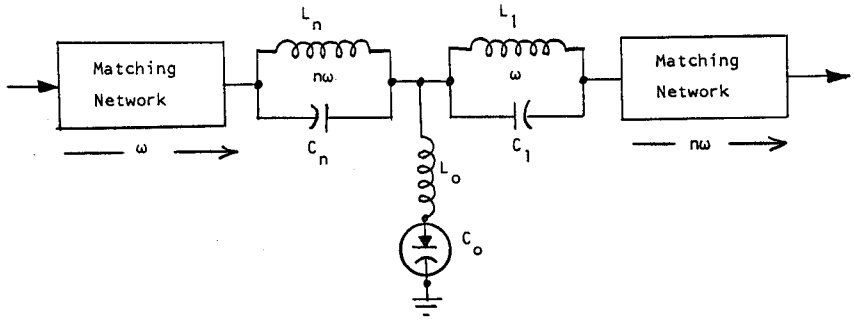
The design approach is summarized as a list of steps that may be followed by the designer: 1) Using TABLE I, select the overall multiplication ratio and the individual multiplier ratios; 2) from Fig. 3 or available references on efficiency, determine the individual power requirements; 3) design the individual multipliers; 4) tune each unit at the expected power input; 5) sequentially add units from the lower frequency and retune the combination at each step; 6) if trouble is experienced, retune individual units; and 7) use of a spectrum analyzer or selective receiver is mandatory at each step to insure signal purity.

TABLE I - Multiplying Ratios Which Use the Fewest Diodes in Doubler, Tripler & Quadrupler Cascades

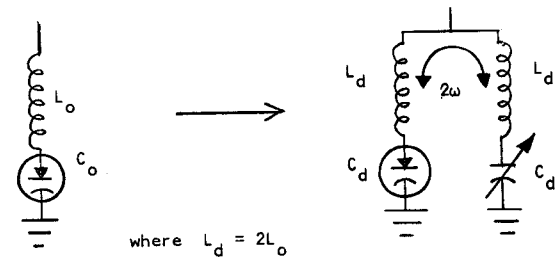
| Multiplication Ratio | Fewest Multiplying Factors | Output Frequency Range Gc (0.1 - 0.2 Gc Input) |
|---|---|---|
| 2 | 2 | 0.2 - 0.4 |
| 3 | 3 | 0.3 - 0.6 |
| 4 | 4 | 0.4 - 0.8 |
| 6 | 2 x 3 | 0.6 - 1.2 |
| 8 | 2 x 4 | 0.8 - 1.6 |
| 9 | 3 x 3 | 0.9 - 1.8 |
| 12 | 3 x 4 | 1.2 - 2.4 |
| 16 | 4 x 4 | 1.6 - 3.2 |
| 18 | 2 x 3 x 3 | 1.8 - 3.6 |
| 24 | 2 x 3 x 4 | 2.4 - 4.8 |
| 27 | 3 x 3 x 3 | 2.7 - 5.4 |
| 32 | 2 x 4 x 4 | 3.2 - 6.4 |
| 36 | 3 x 3 x 4 | 3.6 - 7.2 |
| 48 | 3 x 4 x 4 | 4.8 - 9.6 |
| 64 | 4 x 4 x 4 | 6.4 -12.8 |

TABLE II - Parametric Multiplier Results

| Output Freq. in Mc | Multiplication Ratio | Power Out in Watts | Conversion Loss in db | Diode Used |
|---|---|---|---|---|
| Lumped Design | | | | |
| 100 | 2 | 15.0 | 1.9 | PC117-47 (2) |
| 200 | 2 | 8.0 | 2.7 | PC116-22 (2) |
| 300 | 2 | 1.5 | 1.25 | MA4347E |
| 400 | 2 | 6.0 | 1.3 | PC116-22 (2) |
| 400 | 4 | 7.0 | 4.3 | PC117-47 (2) |
| 400 | 3 | 0.7 | 3.2 | PC115-10 |
| 553 1/3 | 4 | 0.21 | 5.8 | D4252C |
| Coaxial Design | | | | |
| 800 | 2 | 3.2 | 1.9 | MA4348F |
| 1600 | 2 | 0.5 | 3.4 | MA4348C |
| 1600 | 4 | 2.0 | 4.8 | MA4348F |
| 1600 | 4 | 0.21 | 5.3 | MA4348E |
| 3200 | 2 | 0.96 | 3.6 | MA4348B |
| 3200 | 4 | 0.2 | 10.0 | MA4348C |
| 6400 | 4 | 0.18 | 9.8 | D4262D |
| 6400 | 4 | 0.16 | 10.9 | D4260C |
| 6400 | 4 | 0.015 | 11.2 | D4221H |




For tripler or quadrupler operation, modify the circuit as follows:




where $L_d = 2L_o$

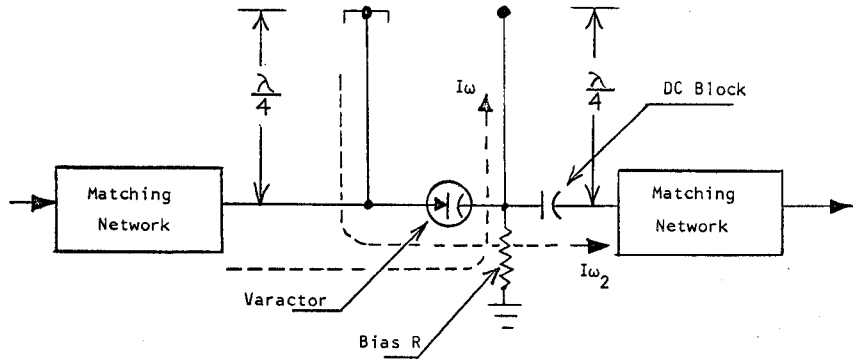
and $C_d = \frac{1}{2}C_o$ = diode capacitance

Table of Element Values

| Element | Doubler | Tripler | Quadrupler |
|---|---|---|---|
| $C_o$ | $C_d$ | $2C_d$ | $2C_d$ |
| $L_o$ | $\frac{1}{2}\omega^2 C_o$ | $\frac{1}{4}\omega^2 C_o$ | $\frac{1}{4}\omega^2 C_o$ |
| $C_1$ | $4C_o/3$ | $9C_o/10$ | $16C_o/45$ |
| $L_1$ | $3L_o/2$ | $40L_o/9$ | $45L_o/4$ |
| $C_n$ | $2C_o/3$ | $C_o/6$ | $4C_o/45$ |
| $L_n$ | $3L_o/4$ | $24L_o/9$ | $45L_o/16$ |

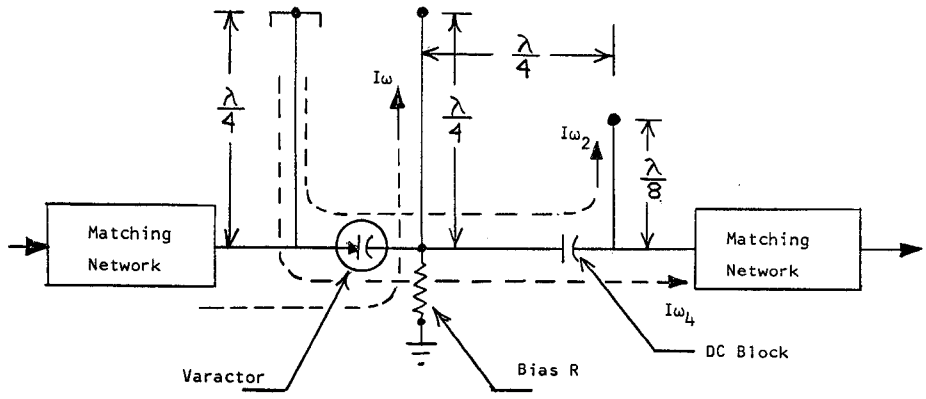
STANDARD MULTIPLIER FOR LUMPED CONSTANT OPERATION

Figure 1.



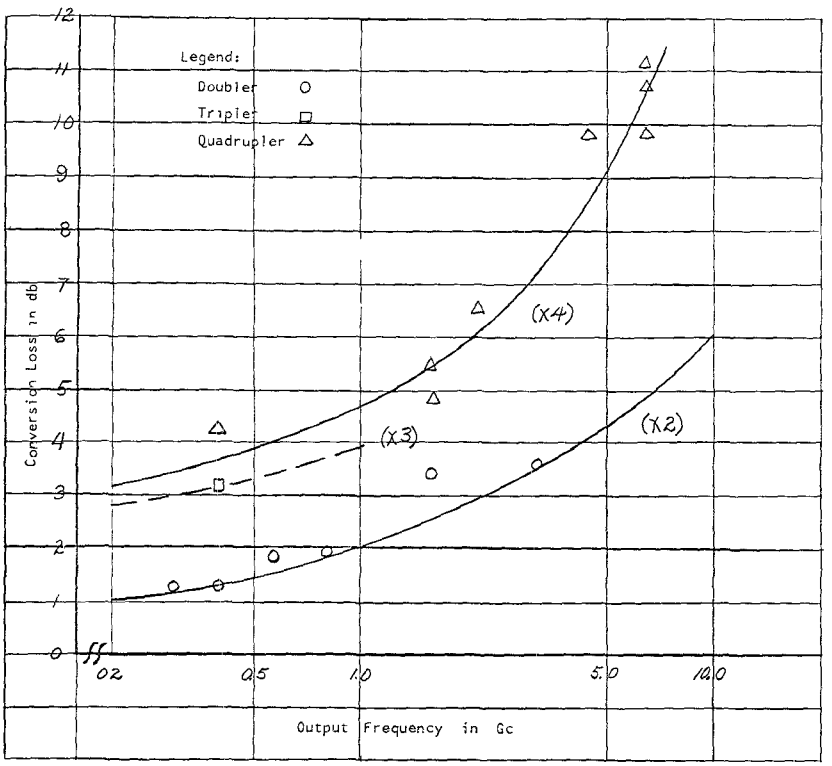

COAXIAL DOUBLER

Figure 2a.




COAXIAL QUADRUPLER

Figure 2b.




MULTIPLIER CONVERSION LOSS VS. FREQUENCY

Figure 3.

# NOTES